2911
PCM CODEC — A LAW
8-BIT COMPANDED A/D AND D/A CONVERTER

- **Per Channel, Single Chip Codec**
- **CCITT G711 and G732 Compatible. Even Order Bits Inversion Included**
- **Microcomputer Interface with On-Chip Time-Slot Computation**
- **66dB Dynamic Range, with Resolution Equivalent to 11-Bit Linear Conversion Around Zero**
- **±5% Power Supplies: +12V, +5V, -5V**
- **On-Chip Voltage Reference**
- **Low Power Consumption: 250 mW. Standby Power: 90 mW**
- **All Digital Inputs and Outputs TTL Compatible**
- **Fabricated with Reliable N-Channel MOS Process**

The Intel® 2911 is a fully integrated PCM (Pulse Code Modulation) Codec (Coder-Decoder), fabricated with N-channel silicon gate technology. The high density of integration allows the sample and hold circuits, the digital-to-analog converter, the comparator and the successive approximation register to be integrated on the same chip, along with the logic necessary to interface a full duplex PCM link.

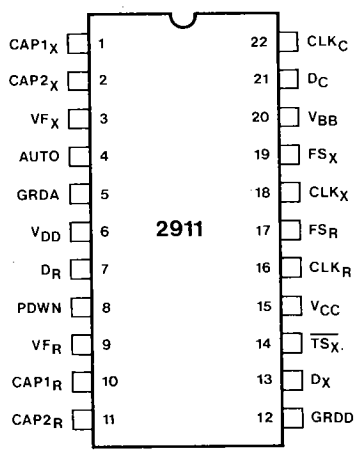
The primary applications are in telephone systems:

- Transmission — 30/32 Channel Systems at 2.048 Mbps
- Switching — Digital PBX's and Central Office Switching Systems
- Concentration — Subscriber Carrier/Concentrators

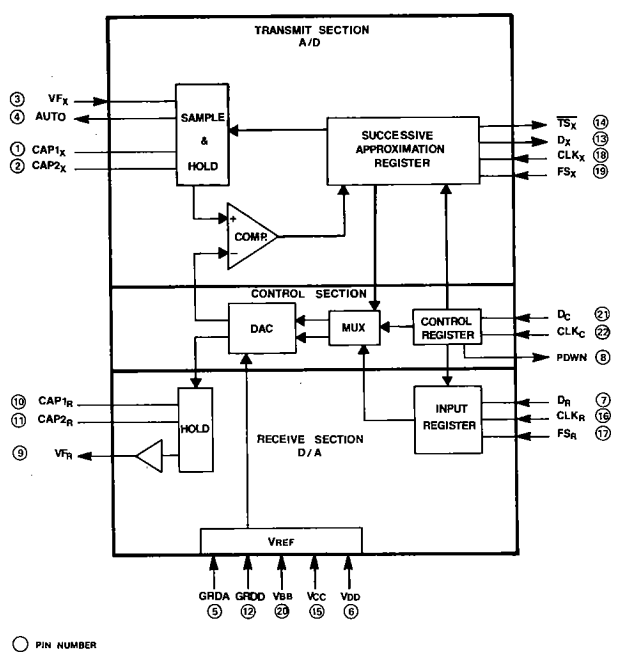
The wide dynamic range of the 2911 (66 dB) and the minimal conversion time (40 μsec minimum) make it an ideal product for other applications, like:

- Data Acquisition
- Telemetry
- Secure Communications Systems
- Signal Processing Systems

PIN CONFIGURATION



BLOCK DIAGRAM



OCTOBER 1977

PIN DESCRIPTION

Pin No.	Symbol	Function	Description
1 2	$CAP1_X$ $CAP2_X$	Hold	Connections for the transmit holding capacitor. For an 8 kHz sampling system the capacitor should be 2000 pF, 20%.
3	VF_X	Input	Analog input to be encoded into a PCM word. The signal on this lead is sampled at the same rate as the transmit frame synchronization pulse FS_X, and the sample value is held in the external capacitor connected to the $CAP1_X$ and $CAP2_X$ leads until the encoding process is completed.
4	AUTO	Output	Most significant bit of the encoded PCM word (+5V for positive, -5V for negative value). Used as an internal ground offset correction, by integrating it through the input coupling capacitor. Refer to the Codec interface section.
5	GRDA	Ground	Analog return common to the transmit and receive analog circuits. Not connected to GRDD internally. The external connection to GRDD should have a very low impedance.
6	V_{DD}	Power	+12V, ±5%, referenced to GRDD or GRDA, depending upon system grounding considerations.
7	D_R	Input	Receive PCM highway (serial bus) interface. The Codec serially receives a PCM word (8-bits) through this lead at the proper time defined by FS_R, CLK_R, D_C, and CLK_C.
8	PDWN	Output	Normally low, this signal goes high while the Codec is in the power down mode. TTL interface, open drain output.
9	VF_R	Output	Analog output. The voltage present on VF_R is the decoded value of the PCM word received on lead D_R. This value is held constant between two conversions. For the dynamic range description, refer to the Codec operation section, decoding paragraph.
10 11	$CAP1_R$ $CAP2_R$	Hold	Connections for the receive holding capacitor. For an 8 kHz sampling system, the capacitor should be 400 pF, 20%.
12	GRDD	Ground	Ground return common to the DC power supplies, optionally V_{BB}, V_{CC}, and V_{DD}.
13	D_X	Output	Output of the transmit side onto the send PCM highway (serial bus). The 8-bit PCM word is serially sent out on this pin at the proper time defined by FS_X, CLK_X, D_C, and CLK_C. TTL three-state output.
14	$\overline{TS_X}$	Output	Normally high, this signal goes low while the Codec is transmitting an 8-bit PCM word on the D_X lead. (Time-slot information used for diagnostic purposes and also to gate the data on the D_X lead.) TTL interface, open drain output.
15	V_{CC}	Power	+5V, ±5%, referenced to GRDD.
16	CLK_R	Input	Master receive clock defining the bit rate on the receive PCM highway. Typically 2.048 Mbps for a carrier system. Maximum rate 2.1 Mbps. 50% duty cycle. TTL compatible.
17	FS_R	Input	Frame synchronization pulse for the receive PCM highway. Maximum repetition rate 16 kHz. For functional description, refer to the Codec operation section, Codec control paragraph. TTL interface.
18	CLK_X	Input	Master transmit clock defining the bit rate on the transmit PCM highway. Typically 2.048 Mbps for a carrier system. Maximum rate 2.1 Mbps. 50% duty cycle. TTL interface.
19	FS_X	Input	Frame synchronization pulse for the transmit PCM highway. Maximum repetition rate 16 kHz. For functional description, refer to the Codec operation section, Codec control paragraph. TTL interface.

Pin No.	Symbol	Function	Description
20	V_{BB}	Power	-5V, ±5%, referenced to GRDD or GRDA, depend-upon system grounding considerations.
21	D_C	Input	Data input to program the Codec for the chosen mode of operation. For functional description, see the Codec operation section, Codec control paragraph. TTL interface.
22	CLK_C	Input	Clock input to clock in the data on the D_C lead in order to define the mode of operation of the Codec. Maximum rate 2.1 Mbps. For functional description, refer to the Codec operation section, Codec control paragraph. TTL interface.

FUNCTIONAL DESCRIPTION

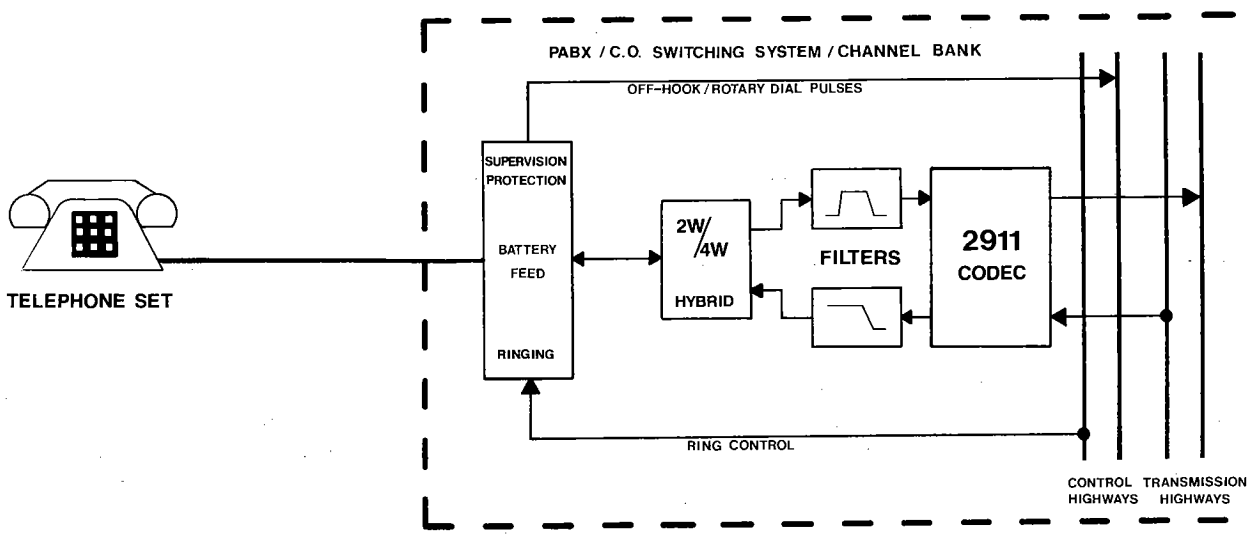
The 2911 PCM Codec provides the analog-to-digital and the digital-to-analog conversions necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system. The Codec is intended to be used on line and trunk terminations.

In a typical telephone system the Codec is located between the PCM highways and the channel filters.

The Codec encodes the incoming analog signal at the frame rate (FS_X) into an 8-bit PCM word which is sent out on the D_X lead at the proper time. Similarly, on the receive link, the Codec fetches an 8-bit PCM word from the receive highway (D_R lead) and decodes an analog value which will remain constant on lead VF_R until the next receive frame. Transmit and receive frames are independent. They can be asynchronous (transmission) or synchronous (switching) with each other.

Circuitry is provided within the Codec to internally define the transmit and receive time-slots in order to minimize the common equipment. This feature can be bypassed and discrete time-slots sent to each Codec within a system.

In the power-down mode, most functions of the Codec are disabled to reduce power dissipation to a minimum.

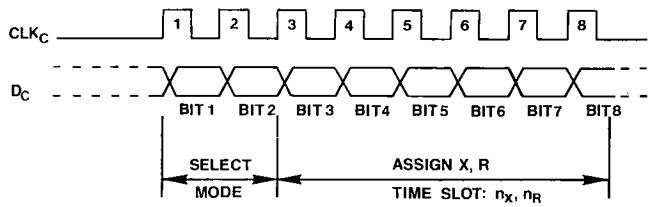


TYPICAL LINE TERMINATION

CODEC OPERATION

Codec Control

The operation of the 2911 is defined by serially loading an 8-bit word through the D_C lead (data) and the CLK_C lead (clock). The loading is asynchronous with the other operations of the Codec, and takes place whenever transitions occur on the CLK_C lead. The D_C input is loaded in during the trailing edge of the CLK_C input.



The control word contains two fields:

Bit 1 and bit 2 define whether the subsequent 6 bits apply to both the transmit and receive side (00), the transmit side only (01), the receive side only (10) or whether the Codec should go into the standby, power-down mode (11).

When coming out of the power down mode, double programming is required with the two 8-bit bursts separated by at least two frames.

The last 6 bits of the control word define the time-slot assignment, from 000000 (time-slot 1) to 111111 time-slot 64).

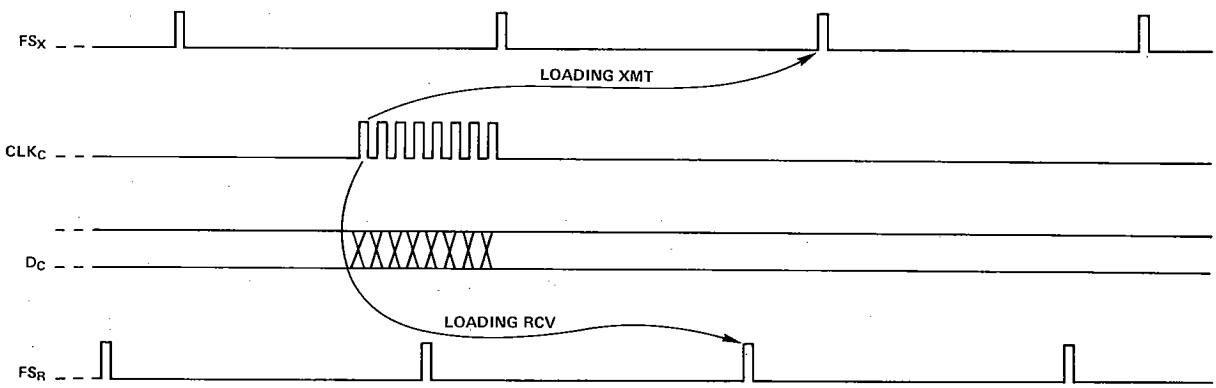
Bit 3 is the most significant bit and bit 8 the least significant and last into the Codec.

Bit 1	Bit 2	Mode
0	0	X & R
0	1	X
1	0	R
1	1	Standby

Bit 3 8	Time Slot
0 0 0 0 0 0	1
0 0 0 0 0 1	2
:	:
:	:
1 1 1 1 1 1	64

The Codec will retain the control word (or words) until a new word is loaded in or until power is lost. This feature allows dynamic allocation of the time-slots for switching applications.

The clocking of a full control word (8 bits) has to take place in less time than the frame duration (elapsed time between two FS_X or FS_R pulses). The Codec will load its transmit and/or receive time-slot control registers upon the occurrence of the second FS (X or R) pulse following a transition on the CLK_C lead.



Time-Slots

A time-slot is a group of eight adjacent clock pulses (X or R) starting with a leading edge of the corresponding CLK (X or R). Time-slot 1 begins with the next leading CLK (X or R) edge following the leading edge of FS (X or R). The time-slots are adjacent (i.e., there is no gap between two consecutive time-slots).

There are two options to run the system timing:

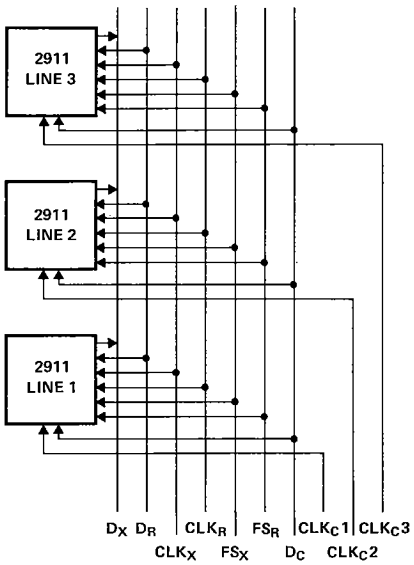
1. Microcomputer Controlled Mode

The same FS_X pulse is sent to all Codecs in the system. Similarly, each Codec receives the same FS_R pulse. Each Codec is programmed for a different time-slot. Each Codec computes its own time-slot, counting down the CLK (X or R) pulses until there is a match with the last 6 bits of the control word. The counts are reset by the FS (X or R) pulse. Thus, there is no need for external generation of the individual time-slot pulses.

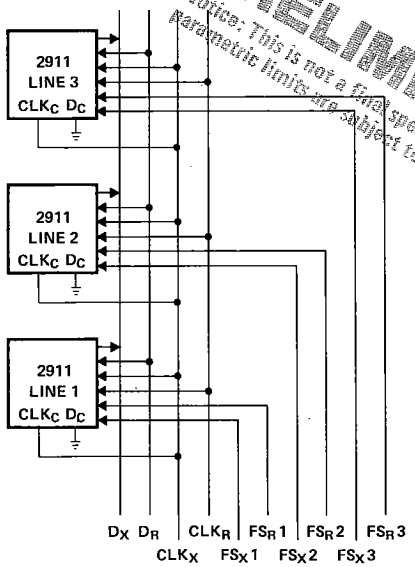
2. Direct Control Mode

Each Codec is programmed for time-slot 1 (code 00000000 for the control word). A different FS_X and FS_R pulse is sent to each Codec, staggered 8 clock pulses apart from Codec to Codec. Each Codec will consider its time-slot to be made of the 8 clock pulses beginning with the next leading CLK (X or R) edge following the leading edge of the FS (X or R) pulses. In the direct mode, there is a need to externally generate a different FS_X and a different FS_R pulse for each Codec.

MICROCOMPUTER CONTROL MODE

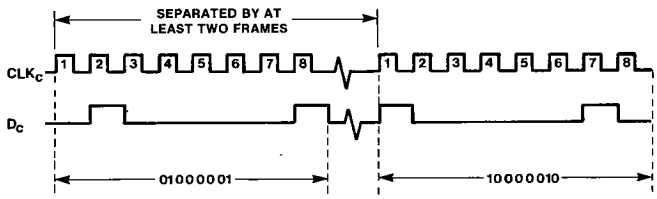


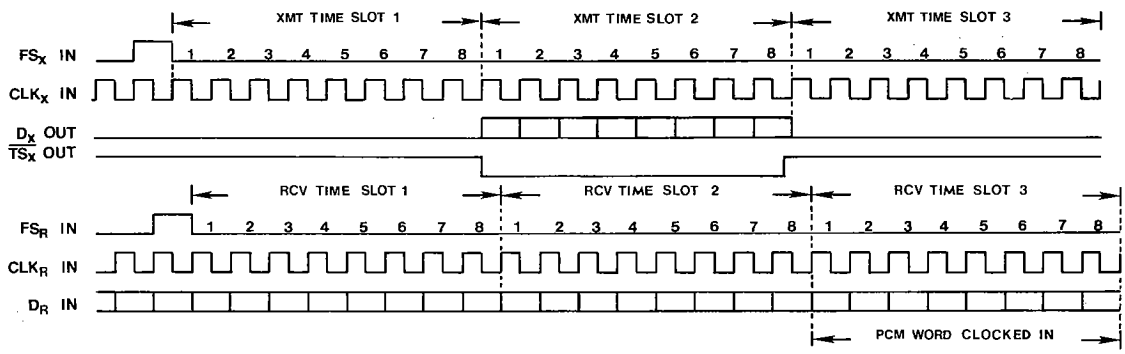
DIRECT MODE



Example:

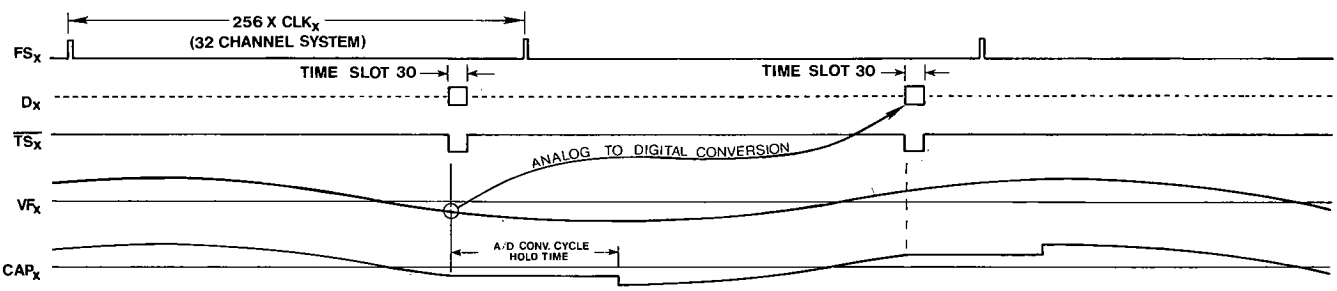
The two words 01000001 and 10000010 have been loaded into the Codec. The transmit side is now programmed for time-slot 2 and the receive side for time-slot 3. The Codec will output a PCM word on the transmit PCM highway (bus) during the time-slot 2 of the transmit frame, and will fetch a PCM word from the receive PCM highway during time-slot 3.





Encoding

The VF signal to be encoded is input on the VF_X lead. An internal switch samples the signal and the hold function is performed by the external capacitor connected to the $CAP1_X$ and $CAP2_X$ leads. The sampling is synchronized with the transmit time-slot and the conversion takes place during the following frame (worst case conversion time is 16 time-slots). The PCM word is then output on the D_X lead at the proper time-slot occurrence of the following frame as described earlier (see Codec control paragraph). The A/D converter saturates at 3.05 volts.



Conversion Law

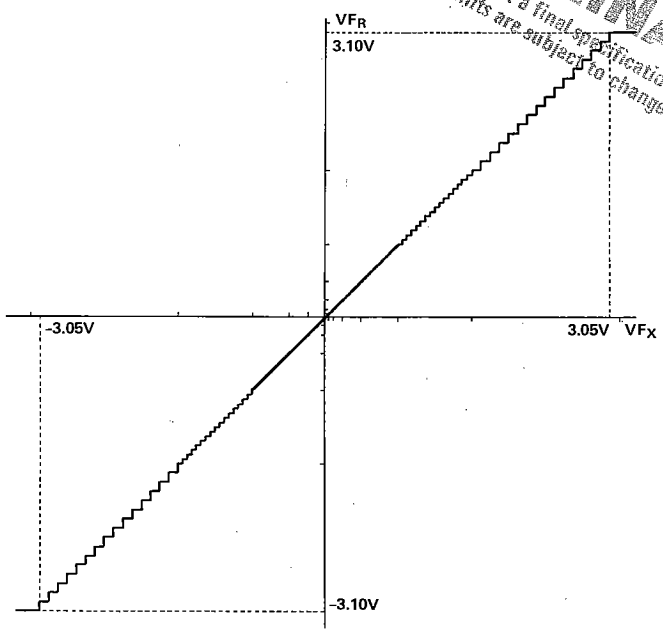
The conversion law is commonly referred to as the A Law.

The Codec provides a piecewise linear approximation of the logrithmic law through 13 segments. Each segment is made of 16 steps with the exception of the first segment which has 32 steps. In adjacent segments the step sizes are in a ratio of two to one. Within each segment, the step size is constant.

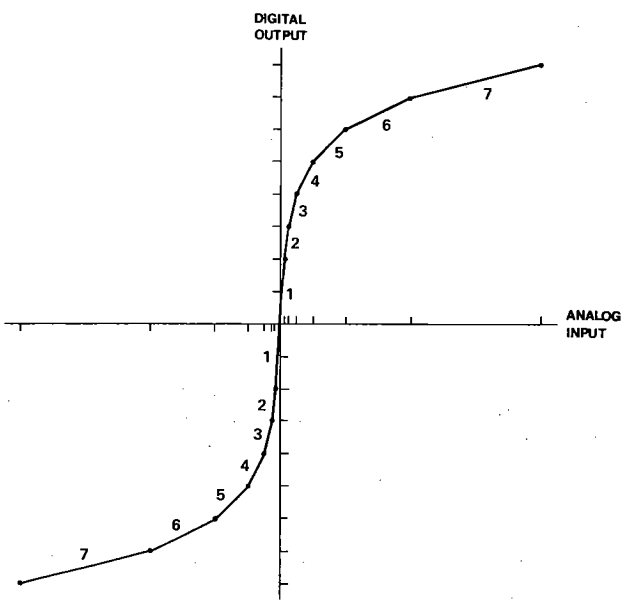
The output levels are midway between the corresponding decision levels. The output levels Y_n are related to the input levels X_n by the expression:

$$Y_n = \frac{X_{n-1} + X_n}{2} \qquad 0 < n \leq 128$$

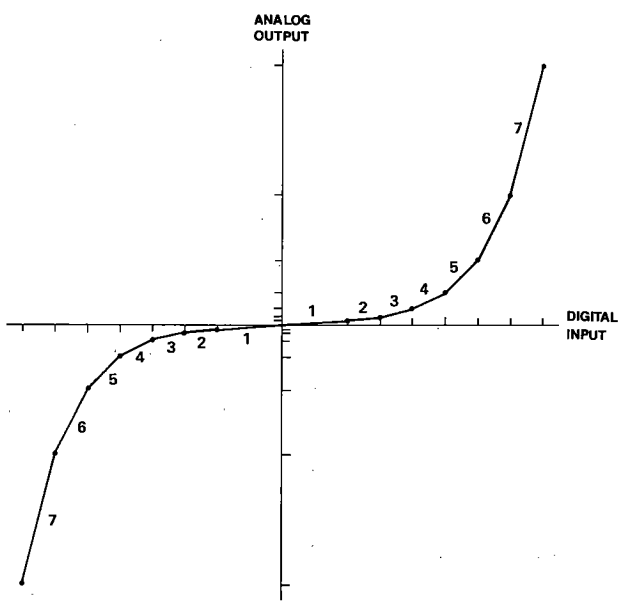
CODEC TRANSFER CHARACTERISTIC



CODER TRANSFER CHARACTERISTIC
(A/D CONVERSION)



DECODER TRANSFER CHARACTERISTIC
(D/A CONVERSION)



A LAW – POSITIVE INPUT VALUES

(For Negative Input Values, Invert Bit 1)

1	2	3	4	5	6	7	8
Segment No.	No. of Steps x Step Size	Value at Segment End Points	Decision Value No. n	Decision Value X_n (1)	PCM Word(4) Bit Number 1 2 3 4 5 6 7 8	Normalized Value at Decoder Output Y_n(5)	Decoder Output Value No.
		4096(3)	(128)	(4096)			
7	16 x 128		127 … 113	3968 … 2176	1 1 1 1 1 1 1 1 … (2)	4032 …	128 …
6	16 x 64	2048	112 … 97	2048 … 1088	1 1 1 1 0 0 0 0 … (2)	2112 …	113 …
5	16 x 32	1024	96 … 81	1024 … 544	1 1 1 0 0 0 0 0 … (2)	1056 …	97 …
4	16 x 16	512	80 … 65	512 … 272	1 1 0 1 0 0 0 0 … (2)	528 …	81 …
3	16 x 8	256	64 … 49	256 … 136	1 1 0 0 0 0 0 0 … (2)	264 …	65 …
2	16 x 4	128	48 … 33	128 … 68	1 0 1 1 0 0 0 0 … (2)	132 …	49 …
1	32 x 2	64	32 … 1	64 … 2	1 0 1 0 0 0 0 0 … (2)	66 …	33 …
			0	0	1 0 0 0 0 0 0 0	1	1

NOTES:

(1) 4096 normalized value units correspond to VF_X max = 3.14 dBmO or 3.15 volts.

(2) The PCM word corresponding to positive input values between two successive decision values numbered n and n+1 (see column 4) is (128+n) expressed as a binary number.

(3) X_{128} is a virtual decision value.

(4) The PCM word on the highways is the same as the one shown in column 6, with the even order bits inverted. The 2911 provides for the inversion of the even order bits on both the send and receive sections. The sign bit is inverted on the encoder side only.

(5) The voltage output on the VF_R lead is equal to the normalized value given in the table, augmented by an offset. The offset value is approximately 15mV.

Decoding

The PCM word fetched from the receive PCM highway is decoded as described in the previous paragraph. The decoded value is held in the external capacitor connected to the $CAP1_R$ and $CAP2_R$ leads. The output signal on lead VF_R has a dynamic range of ±3.10 volts; it is held constant between two successive decode operations. The VF_R output is updated within the fifth time-slot following the receive time-slot in which the channel is operating.

Standby Mode — Power Down

To minimize power consumption and dissipation in large systems, a standby mode is provided by loading a control word (D_C) with a "1" in bits 1 and 2 locations. Most of the Codec functions thereby become disabled, with the exception of the interface to the D_C and CLK_C leads, to allow the Codec to be reactivated.

The power consumption in the standby mode is less than 90 mW.

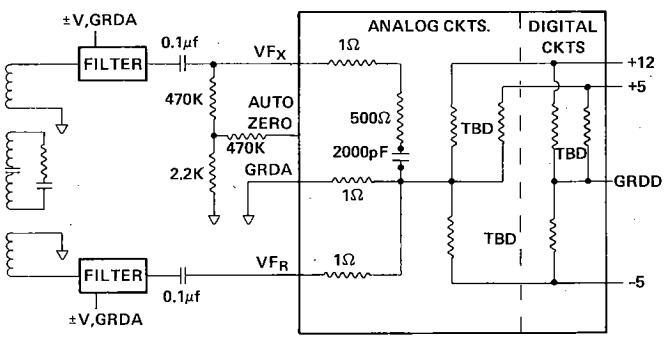
VOLTAGE REFERENCE FOR THE D/A CONVERSION

The voltage reference is generated on-board the chip and is calibrated during the manufacturing process. The tolerance is ±20mV. The dynamic range of the digital-to-analog converter is ±3.10 volts.

APPLICATION — LINE INTERFACE

Grounding

Digital grounding is connected to the GRDD lead. It is the common return for the digital signals.



Analog grounding is connected to the GRDA lead. The GRDA and GRDD lead are not connected inside the 2911. An external connection is thus necessary outside the Codec to tie all the analog ground lines to the common return of the system GRDD. That external connection has to have a minimal impedance to avoid a DC offset in the Codec.

Auto Zero

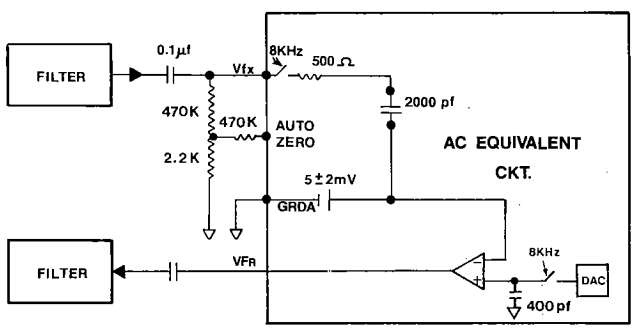
The auto zero output (most significant bit or sign bit of the A/D conversion) integrated over a long time constant will compensate for the DC offset inside the Codec (voltage difference between the bottom of the DAC and GRDA).

The above drawing shows a possible connection between the VF_X and Auto leads.

While improving DC offset, the use of Auto Zero may raise idle channel noise due to biasing near zero with resultant encoder "hunting" of the least significant bit.

Filters Interface

Attached is the schematic of the equivalent circuits of the input and output of the Codec. Note that the output pulse stream is of the non-return to zero type.



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	−40°C to +80°C
Storage Temperature	−65°C to +150°C
Supply Voltage with Respect to V_{SS}	−0.5V to +14V
All Input Voltages	−0.5V to (V_{DD} + 1V)
Outputs	−1V to (V_{DD} + 1V)
Power Dissipation	1.35W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V$, $V_{CC} = 5V$, $V_{BB} = -5V$

POWER DISSIPATION

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Unit	Test Conditions
I_{DDO}	Standby Current		TBD		mA	
I_{CCO}	Standby Current		TBD		mA	V_{DD} = +12, +10%
I_{BBO}	Standby Current		TBD		mA	V_{CC} = 5.0, +10%
						V_{BB} = -5.0, -10%
I_{DDI}	Operating Current		TBD		mA	Clocking Frequency
I_{CCI}	Operating Current		TBD		mA	X & R = 2.048 Mbps
I_{BBI}	Operating Current		TBD		mA	

DIGITAL INTERFACE

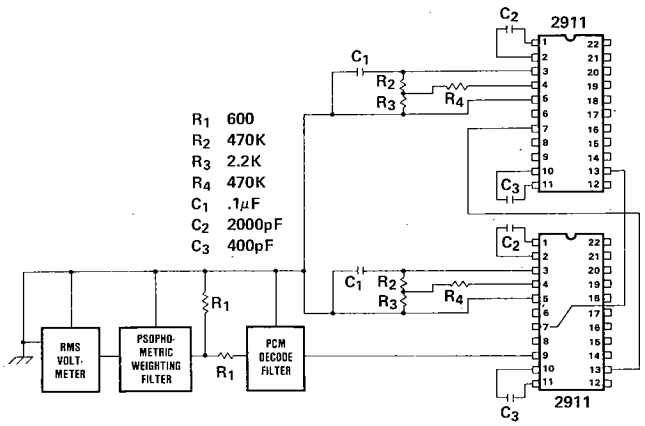
Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Unit	Test Conditions
I_{IL}	Low Level Input Current			10	μA	$V_{IN} < V_{IL}$
I_{IH}	High Level Input Current			10	μA	$V_{IN} > V_{IH}$
V_{IL}	Input Low Voltage			+0.8	V	
V_{IH}	Input High Voltage	+2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 10 mA on D_X 6.4 mA on $\overline{TS_X}$
V_{OH}	Output High Voltage	2.4			V	I_{OH} = 30 mA on D_X

ANALOG INTERFACE

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Unit	Test Conditions
A_{IL}	Input Leakage when Sampling			1	μA	$-3.1V < V_{IN} < 3.1V$
A_{IZ}	Input Impedance when Sampling			500	Ω	In series with CAP_X to GRD
A_{OZ}	Output Impedance	1.8	2.0	2.2	kΩ	
A_{OR}	Dynamic Range (VF_R)	-3.1		+3.1	V	±10 mV
N_{IC}	Idle Channel Noise			-72	dBmOp	
ΔG	Gain Tracking Deviation from Gain at 0dBmO			±0.3 ±0.6 ±2.0	dB dB dB	Signal Level +3dBmO to -40dBmO Signal Level -40dBmO to -50dBmO Signal Level -50dBmO to -55dBmO
S/D	Signal to Total Distortion Ratio			35 29 24	dB dB dB	Signal Level 0dBmO to -30dBmO Signal Level -40dBmO to -45dBmO Signal Level -45dBmO

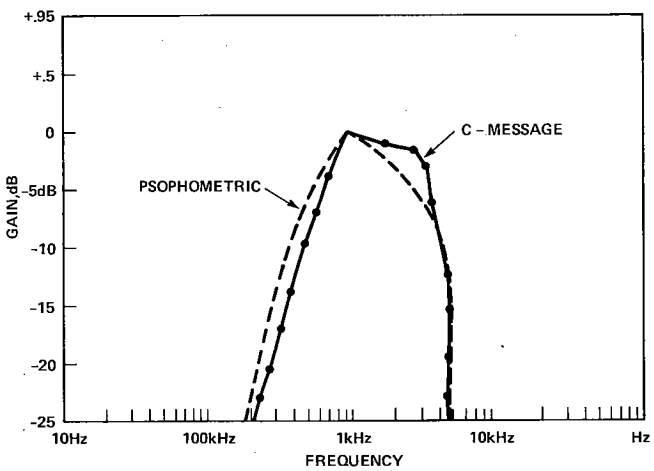
Test Circuit Idle Channel Noise

IDLE CHANNEL NOISE TEST CIRCUIT



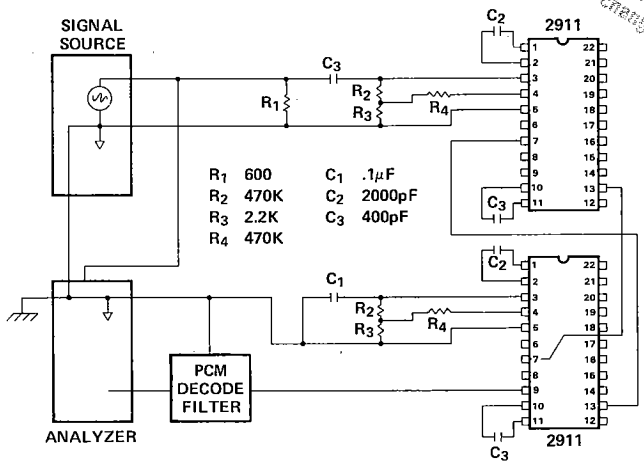
Both codecs are operated under idle channel conditions. The PCM decode filter meets the CCITT G712 recommendation; its own idle channel noise is less than -78 dB mop. The Psophometric weighting curve to be used for the test is given below.

C-MSG AND PSOPHOMETRIC WEIGHTING CURVES



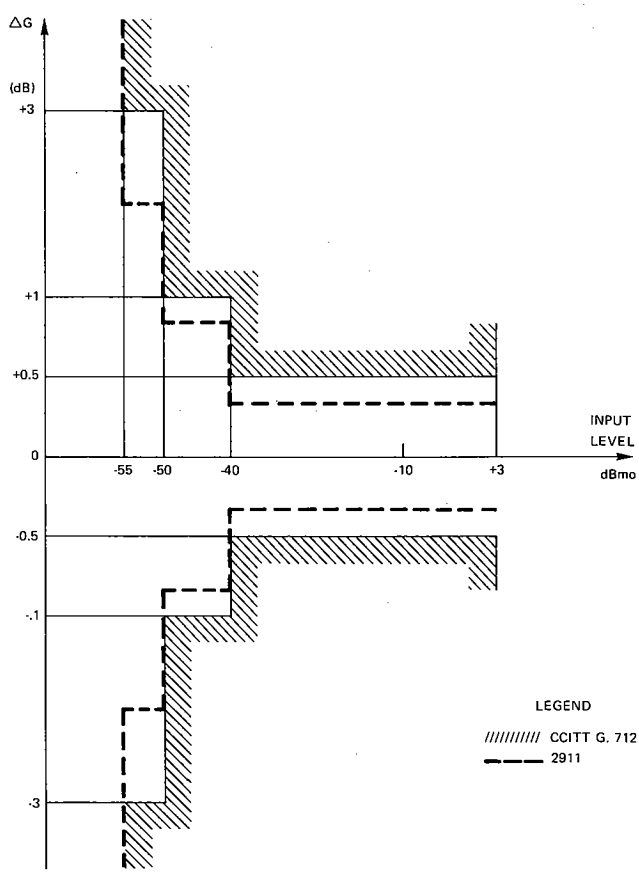
Test Circuit — Gain Tracking

GAIN TRACKING TEST CIRCUIT



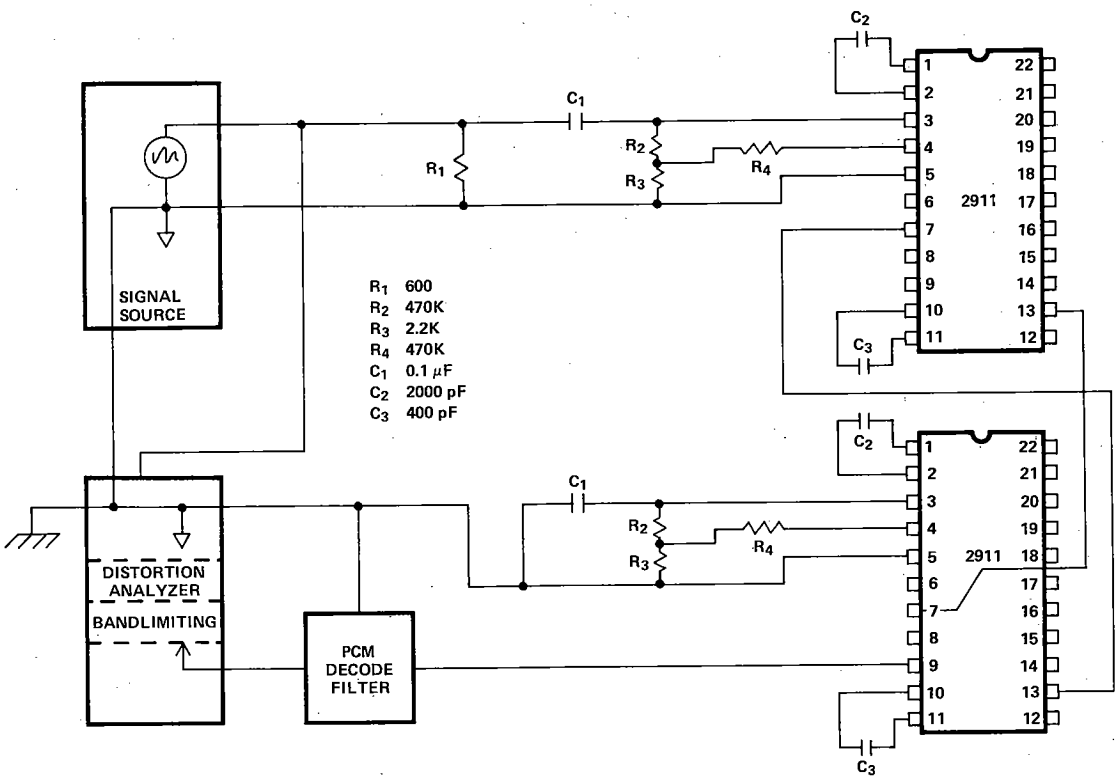
The test signal is sinusoidal at 1.020kHz. The PCM decode filter must compensate for the $\frac{\sin x}{x}$ distortion introduced by the non-return to zero output of the codec. The gain tracking of that filter must be factored out if it is of similar magnitude to the codec's. The analyzer is a spectrum analyzer, a DC wave analyzer or a network analyzer.

GAIN VARIATION (ΔG) VS. SIGNAL LEVEL
REFERENCE LEVEL 0dBmO



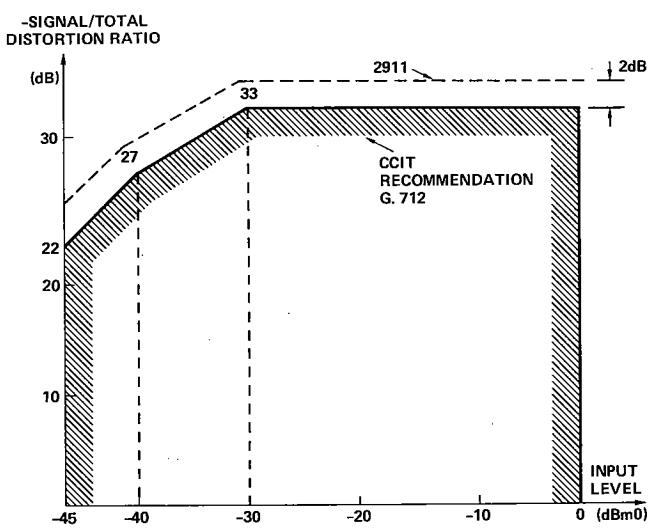
Test Circuit — Signal to Total Distortion S/D

SIGNAL-TO-TOTAL DISTORTION (S/D) TEST CIRCUIT

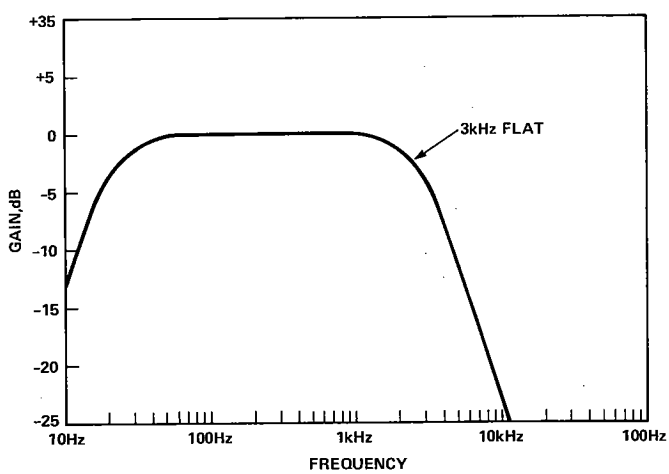


The test signal is sinusoidal at 1.020kHz; the noise weighting is 3kHz flat. The PCM decode filter must compensate for the $\frac{\sin x}{x}$ distortion introduced by the sample and hold circuit in the output stage of the codec. Shown below is the 3kHz weighting curve of the HP 3551 transmission test set.

-SIGNAL/TOTAL DISTORTION RATIO



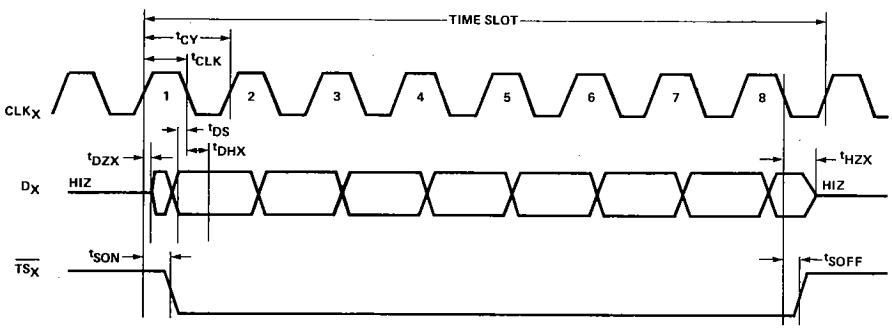
3kHz FLAT AND PROGRAM WEIGHTING CURVES (HP 3551)

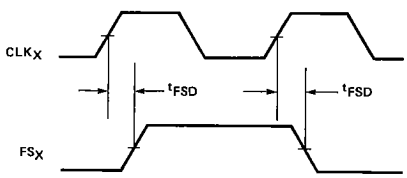


TIMING SPECIFICATION

TRANSMIT SECTION

Symbol	Parameter	Limits		Units	Comments
		Min	Max		
t_{CY}	Clock Period (2.048 MHz Systems)	485		ns	
t_r, t_f	Clock Rise and Fall Time		30	ns	
t_{CLK}	Clock Pulse Width	230		ns	Nominal 50% duty cycle
t_{DS}	New Data Setup	50		ns	Increase by 0.1 ns/pF below 500 pF
t_{DHX}	Data Hold Time	75		ns	
t_{HZX}	Data Float on TS Exit	75	205	ns	
t_{SOFF}	Time Slot X to Disable	70	185	ns	
t_{DZX}	Data Enabled on TS Entry	35		ns	
t_{SON}	Time Slot X to Enable	30	180	ns	
t_{FSD}	Frame Sync Delay	10	100	ns	





RECEIVE AND CONTROL SECTIONS

Symbol	Parameter	Limits		Unit	Comments
		Min	Max		
t_{VFR}	Analog Output Update		7	Time Slot	From the trailing edge of the channel time slot
t_{DSR}	Receive Data Setup	20		ns	
t_{DHR}	Receive Data Hold	50		ns	
t_{DSC}	Control Data Setup	50		ns	
t_{DHC}	Control Data Hold	50		ns	
t_{FSD}	Frame Sync Delay	10	100	ns